AMENDMENTS TO THE CLAIMS

The following is a complete, marked-up listing of revised claims with a status identifier in parenthesis, underlined text indicating insertions, and strikethrough and/or double-bracketed text indicating deletions.

LISTING OF CLAIMS

1. (Previously Presented) A processor having a processor core and at least one peripheral device, comprising:

a selecting circuit for determining at least one of operation states and operating frequencies of a high-speed control circuit and a low-speed and low-power control circuit based on direct monitoring of the high-speed control circuit and the low-speed and low-power control circuit and for outputting a selection signal based on the determination;

the high-speed control circuit for controlling high-speed operations of at least one of the processor core and the peripheral device in response to the selection signal; and

the low-speed and low-power control circuit for controlling low-speed and low-power operations of at least one of the processor core and the peripheral device in response to the selection signal.

2. (Previously Presented) The processor of claim 1, wherein the high-speed control circuit controls the high-speed operations of one of at least the processor core and the peripheral device if the determination indicates the processor is operating in a normal mode, and the low-speed and low-power control circuit controls the low-speed and low-power operations of one of at least the processor core and the peripheral device if the determination indicates the processor is operating in a slow mode.

3. (Previously Presented) The processor of claim 1, wherein the selecting circuit compares an operating frequency of the processor with a predetermined threshold frequency to obtain a compared result and outputs the selection signal based on the compared result.

4. (Original) The processor of claim 3, wherein the high-speed control circuit controls the high-speed operations of one of at least the processor core and the peripheral device when the operating frequency of the processor is higher than the predetermined threshold frequency, and the low-speed and low-power control circuit controls the low-speed and low-power operations of one of at least the processor core and the peripheral device when the operating frequency of the processor is lower than the predetermined threshold frequency.

5. (Original) The processor of claim 1, wherein the processor core is a central processing unit (CPU).

6. (Original) The processor of claim 1, wherein the peripheral device is at least one of a wireless LAN card, a PC card, and a liquid crystal display (LCD).

7. (Previously Presented) A processor having a processor core and peripheral device, comprising:

a selecting circuit for evaluating at least one of operation states and operating frequencies of a high-speed control circuit and a low-speed and low-power control circuit based on direct monitoring of the high-speed control circuit and the low-speed and low-power control circuit and for outputting a selection signal based on the evaluation;

the high-speed control circuit for controlling respective high-speed operations of the processor core and the peripheral device;

the low-speed and low-power control circuit for controlling respective low-speed and low-power operations of the processor core and the peripheral device; and

a multiplexer for, in response to the selection signal, interfacing one of the high-speed control circuit with the processor core and the peripheral device and the low-speed and low-power control circuit with the processor core and the peripheral device.

8. (Previously Presented) The processor of claim 7, wherein the high-speed control circuit controls the high-speed operations of the processor core and the peripheral device if the evaluation indicates the processor is operating in a normal mode, and the low-speed and low-power control circuit controls the low-speed and low-power operations of the processor core and the peripheral device if the evaluation indicates the processor is operating in a slow mode.

9. (Previously Presented) The processor of claim 7, wherein the high-speed control circuit controls the high-speed operations of the processor core and the peripheral device when an operating frequency of the processor higher than a predetermined threshold frequency, and the low-speed and low-power control circuit controls the low-speed and low-power operations of the processor core and the peripheral device when the operating frequency of the processor is lower than the predetermined threshold frequency.

10. (Previously Presented) A processor, comprising:

a circuit for selecting a control circuit from a plurality of control circuits based on direct monitoring of at least one of operation states and operating frequencies of the plurality of control circuits, the control circuit for controlling one of at least a first device and a second device.

11. (Original) The processor of claim 10, further comprising an interface device for interfacing the selected control circuit with at least one of the first device and the second device.

12. (Original) The processor of claim 10, wherein the circuit for selecting compares an operating frequency of the processor to a threshold value in a process of selecting the control circuit from the plurality of control circuits.

13. (Original) The processor of claim 12, wherein the circuit for selecting selects a first control circuit of the plurality of control circuits when the operating frequency is higher than the threshold value.

14. (Original) The processor of claim 13, wherein the circuit for selecting selects a second control circuit of the plurality of control circuits when the operating frequency is lower than the threshold value.

15. (Original) The processor of claim 10, wherein the circuit for selecting evaluates a mode of the processor in a process of selecting the control circuit from the plurality of control circuits.

16. (Original) The processor of claim 15, wherein the circuit for selecting selects a first control circuit of the plurality of control circuits when the mode is a normal mode.

17. (Original) The processor of claim 15, wherein the circuit for selecting selects a second control circuit of the plurality of control circuits when the mode is a slow mode.

18. (Original) The processor of claim 15, wherein the plurality of control circuits includes at least a high-speed control circuit and a low-speed and low-power control circuit.

19. (Original) The processor of claim 15, wherein the first device is a processor core and the second device is a peripheral device.

20. (Previously Presented) A method, comprising:

selecting a control circuit from a plurality of control circuits based on direct monitoring of at least one of operation states and operating frequencies of the plurality of control circuits; and

controlling at least a first device and a second device with the selected control circuit.

21. (Previously Presented) The processor of claim 1, wherein the high-speed control circuit is in an active state before the selecting circuit makes the determination if the determination indicates to output the selection signal to select the high-speed control circuit.

End of Claims Listing